

Claims

- 1 1. Circuit arrangement comprising:
 - 2 - first chips, which each contain a transistor and are arranged along a first axis on a
 - 3 first metallic body in a side-by-side and interspaced manner and are electrically
 - 4 connected to the first body,
 - 5 - second chips, which each contain a transistor and are arranged along a second axis
 - 6 parallel to the first axis on a second metallic body in a side-by-side and
 - 7 interspaced manner and are electrically connected to the second body,
 - 8 - wherein the second chips, with regard to a third axis perpendicular to the first
 - 9 axis, each being arranged opposite an area of the first body, which is located
 - 10 between adjacent first chips,
 - 11 - wherein the second chips each being electrically connected to the corresponding
 - 12 opposite area of the first body via at least one bonding connection,
 - 13 - wherein the first chips, with regard to the third axis each being arranged opposite
 - 14 an area of the second body, which is located between adjacent second chips,
 - 15 - a third metallic body being arranged on the second body so that it is electrically
 - 16 insulated and having projections, each of which being arranged on one of the
 - 17 areas of the second body, and
 - 18 - wherein the first chips each being electrically connected to the opposite projection
 - 19 of the third body via at least one bonding connection.
- 1 2. Circuit arrangement according to Claim 1, wherein
 - 2 - the first body being connected to an output terminal,
 - 3 - the second body being connected to a voltage terminal, and
 - 4 - the third body being connected to a ground terminal.

- 1 3. Circuit arrangement according to Claim 1, wherein
2 - the first chips without packaging being directly mounted on the first body in such
3 a way that an electrical contact is created between the first chips and the first
4 body, and
5 - the second chips without packaging being directly mounted on the second body in
6 such a way that an electrical contact is created between the second chips and the
7 second body.
- 1 4. Circuit arrangement according to Claim 2, wherein
2 - the first chips without packaging being directly mounted on the first body in such
3 a way that an electrical contact is created between the first chips and the first
4 body, and
5 - the second chips without packaging being directly mounted on the second body in
6 such a way that an electrical contact is created between the second chips and the
7 second body.
- 1 5. Circuit arrangement according to Claim 1, further comprising:
2 - a first control line running parallel to the first axis and being connected to the first
3 chips via bonding connections,
4 - a second control line running parallel to the first axis and being connected to the
5 second chips via bonding connections.
- 1 6. Circuit arrangement according to Claim 2, further comprising:
2 - a first control line running parallel to the first axis and being connected to the first
3 chips via bonding connections,
4 - a second control line running parallel to the first axis and being connected to the
5 second chips via bonding connections.

- 1 7. Circuit arrangement according to Claim 3, further comprising:
 - 2 - a first control line running parallel to the first axis and being connected to the first
 - 3 chips via bonding connections,
 - 4 - a second control line running parallel to the first axis and being connected to the
 - 5 second chips via bonding connections.

- 1 8. Circuit arrangement according to Claim 4, further comprising:
 - 2 - a first control line running parallel to the first axis and being connected to the first
 - 3 chips via bonding connections,
 - 4 - a second control line running parallel to the first axis and being connected to the
 - 5 second chips via bonding connections.

- 1 9. Circuit arrangement comprising:
- 2 - a first metallic body,
- 3 - a second metallic body arranged coplanar with said first metallic body,
- 4 - first chips, which each contain a transistor and are arranged along a first axis on
- 5 the first metallic body and are electrically connected to the first body,
- 6 - second chips, which each contain a transistor and are arranged along a second axis
- 7 parallel to the first axis on the second metallic body and are electrically connected
- 8 to the second body,
- 9 - wherein the first and second chips are arranged alternative with respect to the first
- 10 and second axis,
- 11 - wherein the second chips each being electrically connected to the corresponding
- 12 opposite area of the first body via at least one bonding connection,
- 13 - a third metallic body being arranged on the second body so that it is electrically
- 14 insulated and having projections, each of which being arranged on one of the
- 15 areas of the second body, and
- 16 - wherein the first chips each being electrically connected to the opposite projection
- 17 of the third body via at least one bonding connection.
- 1 10. Circuit arrangement according to Claim 9, wherein
- 2 - the first body being connected to an output terminal,
- 3 - the second body being connected to a voltage terminal, and
- 4 - the third body being connected to a ground terminal.
- 1 11. Circuit arrangement according to Claim 9, wherein
- 2 - the first chips without packaging being directly mounted on the first body in such
- 3 a way that an electrical contact is created between the first chips and the first
- 4 body, and
- 5 - the second chips without packaging being directly mounted on the second body in
- 6 such a way that an electrical contact is created between the second chips and the
- 7 second body.

- 1 12. Circuit arrangement according to Claim 10, wherein
2 - the first chips without packaging being directly mounted on the first body in such
3 a way that an electrical contact is created between the first chips and the first
4 body, and
5 - the second chips without packaging being directly mounted on the second body in
6 such a way that an electrical contact is created between the second chips and the
7 second body.

- 1 13. Circuit arrangement according to Claim 9, further comprising:
2 - a first control line running parallel to the first axis and being connected to the first
3 chips via bonding connections,
4 - a second control line running parallel to the first axis and being connected to the
5 second chips via bonding connections.

- 1 14. Circuit arrangement according to Claim 10, further comprising:
2 - a first control line running parallel to the first axis and being connected to the first
3 chips via bonding connections,
4 - a second control line running parallel to the first axis and being connected to the
5 second chips via bonding connections.

- 1 15. Circuit arrangement according to Claim 11, further comprising:
2 - a first control line running parallel to the first axis and being connected to the first
3 chips via bonding connections,
4 - a second control line running parallel to the first axis and being connected to the
5 second chips via bonding connections.

- 1 16. Circuit arrangement according to Claim 12, further comprising:
2 - a first control line running parallel to the first axis and being connected to the first
3 chips via bonding connections,
4 - a second control line running parallel to the first axis and being connected to the
5 second chips via bonding connections.